Documentation

DDS Signal Generator

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Document information

Info	Content
Keywords	AD9832, DDS, signal generator
Abstract	This document describes a small signal generator with either AD9832 or AD9845. These chips are signal generators that use the DDS (digital direct synthesis) method to create output frequencies with very small stepsize. In addition a small control software is described that features setting frequency. An example of creating a WSPR beacon is included as well.

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1 Introduction

This document describes a small DDS signal generator circuit that can be equipped with Analog Devices AD9832 or AD9835 DDS signal generator ICs. The PCB was designed to fit into a small shortwave transceiver but can be used for another purpose as well. One can be to replace a low frequency crystal.

The signal generator circuit does not include any circuit for programming from PC or a microcontroller. This is in order to be flexible regarding the target usage. The all control signals are connected to pin headers instead.

The circuit is inspired by the MiniDDS from SMxxx (URL: http://home4.swipnet.se/w̃-41522/minidds/minidds.html).

2 Description of the circuit

The signal generator circuit can be equiped with two different DDS generator ICs. Therefore the both versions allow different output frequency ranges. With AD9832 the generation of a proper output signal up to 12MHz should be possible. With AD9835 and a different harmonic rejection filter the frequency range extends up to 22MHz.

The circuit needs to be fed with a stable 5V supply voltage. There is no regulator available at the board since 5V are usually available in the most systems. The reference signal is generated by a 5V TTL oszillator. This is a 12x12mm type but a 12x20mm type might fit with some modifications. The reference clock should be between 24MHz and 30MHz (nominal 25MHz) for AD9832 and between 50MHz and 60MHz for AD9835. The clock from the generator can be divided by 4 with the HC241 flip flop. Dividing by two, 8 or 16 can be done after modifying the PCB. The divided clock signal is available at the pin header in order to supply further circuits like a controlling microcontroller. The reference is also fed to the DDS generator IC.

The 5V from the pin header are supplied to the digital section of AD9832 and to the clock divider IC. The analog sections of AD9832 as well as the output amplifier are fed via a decoupling coil.

All control signals (Clock, Data, Chip select, PSel0, PSel1, Fselect) are connected to pin headers. There are no pullup or pulldown resistors available. Consider this fact when programmin control software (use the correct register settings).

The RF output signal from AD9832 is fed to a harmonic filter circuit that should remove unwanted spurious signals that occure if the output is tuned to a frequency close to the maximum output frequency. It is a third order filter. It is important if you want to use a

reference frequency significantly lower than 25MHz. The values for different filter frequencies are described later on.

After passing the filter the RF signal is amplified with a MAX4012 wideband operational amplifier. After the amplifier around +5dBm (around 3mW) at 50Ohm are delivered to a SMA connector. This is sufficient to drive most active RF circuits.

Figure 1 gives an impression of the circuit.

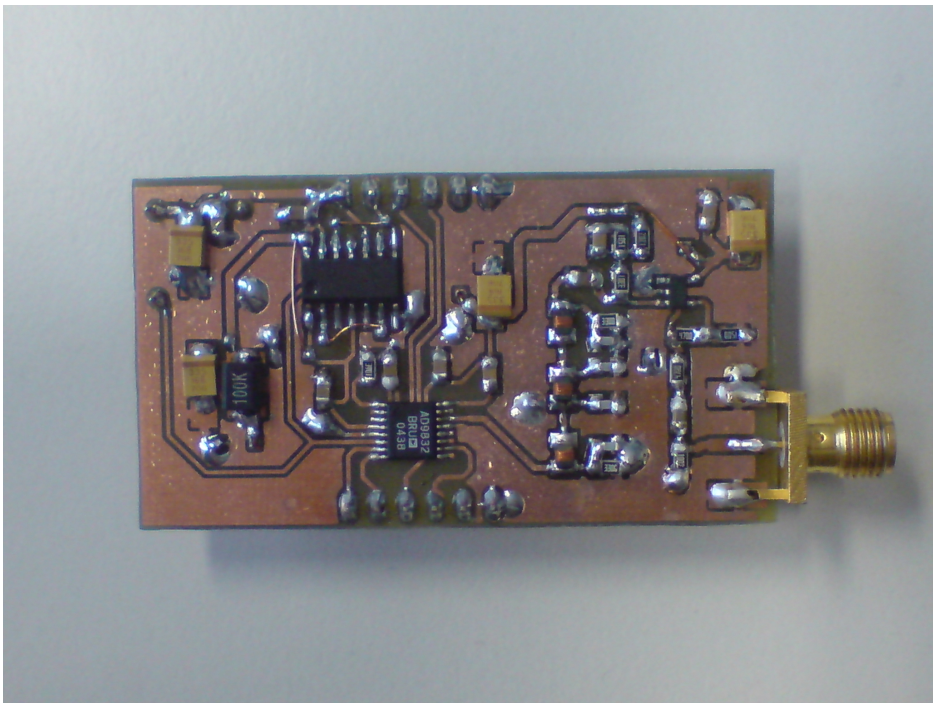

Figure 1: Top view at MiniDDS signal generator

3 Errata

The power supply for the MAX4012 is not connected accordingly in the datasheet. The power supply for this IC needs to be connected to +5V/1 instead of +5V. This means do not assemble the wire at the backside of the PCB but assemble a short connection between C5 and R10 as it can be seen in figure 1.
Furthermore you need to add a ground connection to the board. The groundplane left of the low pass filter is not connected. Thrill a hole through the PCB and solder the ground plan with the common ground at the second side of the PCB.

4 Assembly

The circuit is carried out as double-sided PCB. The second side mainly acts as ground layer and contains power supply routing. In order to make the manufacturing of the PCB more easy it is also possible to etch the top side only. The remaining traces can be easily carried out with small wire connections.
These are between pin 14 and pin 1 of the HC74 and between pin 2 and pin 6 of the HC74 as well as between 8 and 12 of the HC74.
According to the errata connect the positive side of C10 to +5V/1 at R10.

It is recommended to start the assembly of the circuit with soldering all necessary connections between top layer ground and common ground at the bottom layer. Continue at the reference clock and clock divider circuit. This part can be tested separately. After that the DDS itself and the parts around can be assembled. After that you might do another test checking the functionality of the IC. When the DDS generator works assemble the anti-aliasing filter and the amplifier circuit.

See figure 3 for assembly plan.

5 List of components

See table 1 for the list of components.

6 Filter component values

See table 2 for component values of different filter frequencies.

7 Example software for AVR controller

This project includes a small piece of software for the Atmel AVR controller family. This software is written in C and can be used to controll the AD9832/35 DDS via software generated SPI. It can be compiled for various controllers of the AVR family. This will need some changes of register names if you do not use a Atmega644 controller on which this software was tested. The desired output frequency of the signal generator can be entered as a decimal number at a serial terminal connected to the AVR. The parameters are 19k2 8N1. Please see the sourcecode as an example or starting point for your own eperiments. The reference clock frequency used for the DDS IC has to be entered in the AD9832.h header file. There is also a preprocessor define for a default frequency that is set after the start of the microcontroller. This might be used for setting up the generator without the need of external interfacing. If a frequency 0 is entered the signal of the DDS will be off. This can be used to switch off the output of the generator. Please note that there is no error check for the inputs you make except the conversion of the console input to a decimal representation.

8 WSPR beacon generation

In the sourcecode you will find some code fragments that can be used to generate a WSPR (weak signal propagation reporting) beacon signal. The source code is currently hard coded for a reference frequency of 24MHz. Therefore you have to adapt the frequency offset values for the 4-FSK manually. The beacon is generated every 4 slots (each 2 minutes). The timing is derived from the microcontroller reference clock. The divider settings are set matching to 16MHz reference clock. You have to optimize these settings for your crystal in order to reach a minimum timing drift over a long term.
Keep in mind that the software was written for Atmega644 and it will need some changes to register names to get it running for another controller from the AVR family.

Table 1: MiniDDS list of components

Number	Partname	Description
JP1	1x6 header 2.54mm	supply and clock header
JP2	1x6 header 2.54mm	control header
QG1	Oscillator	crstal controlled oscillator 12x12mm
IC1	HC74D	SMD D-flipflop
IC2	AD9832BRU	Analog Devices DDS signal generator
IC3	MAX4012EUK	Maxim Wideband OpAmp
C1,C3,C8,C9,C17,C18	100nF	Ceramic 0805
C2,C5,C6,C7	4.7uF	Tantal
C10,C11	10nF	Ceramic 0805
C4,C16	1uF	Ceramic 0805
L1	10mH	ferrite beat
R1	47Ω	0805
R2	470Ω	0805
R3	150Ω	0805
R4,R10	10kΩ	0805
R5	3.9kΩ	0805
R6,R7	330Ω	0805
R8	1.5kΩ	0805
R9	3.3kΩ	0805
C12,C13,C14,C15	see table 2	Ceramic 0805
L2,L3,L4	see table 2	Inductance

Table 2: LP filter component values

Component	6MHz	12MHz	25MHz
C12	82pF	52pF	22pF
C13	180pF	100pF	47pF
C14	180pF	100pF	47pF
C15	82pF	52pF	22pF
L2	10uH	5.6uH	3.3uH
L3	12uH	6.8uH	3.9uH
L4	10uH	5.6uH	3.3uH

9 Schematic

See figure 2

10 Assembly Plan

See figure 3 for assembly plan.

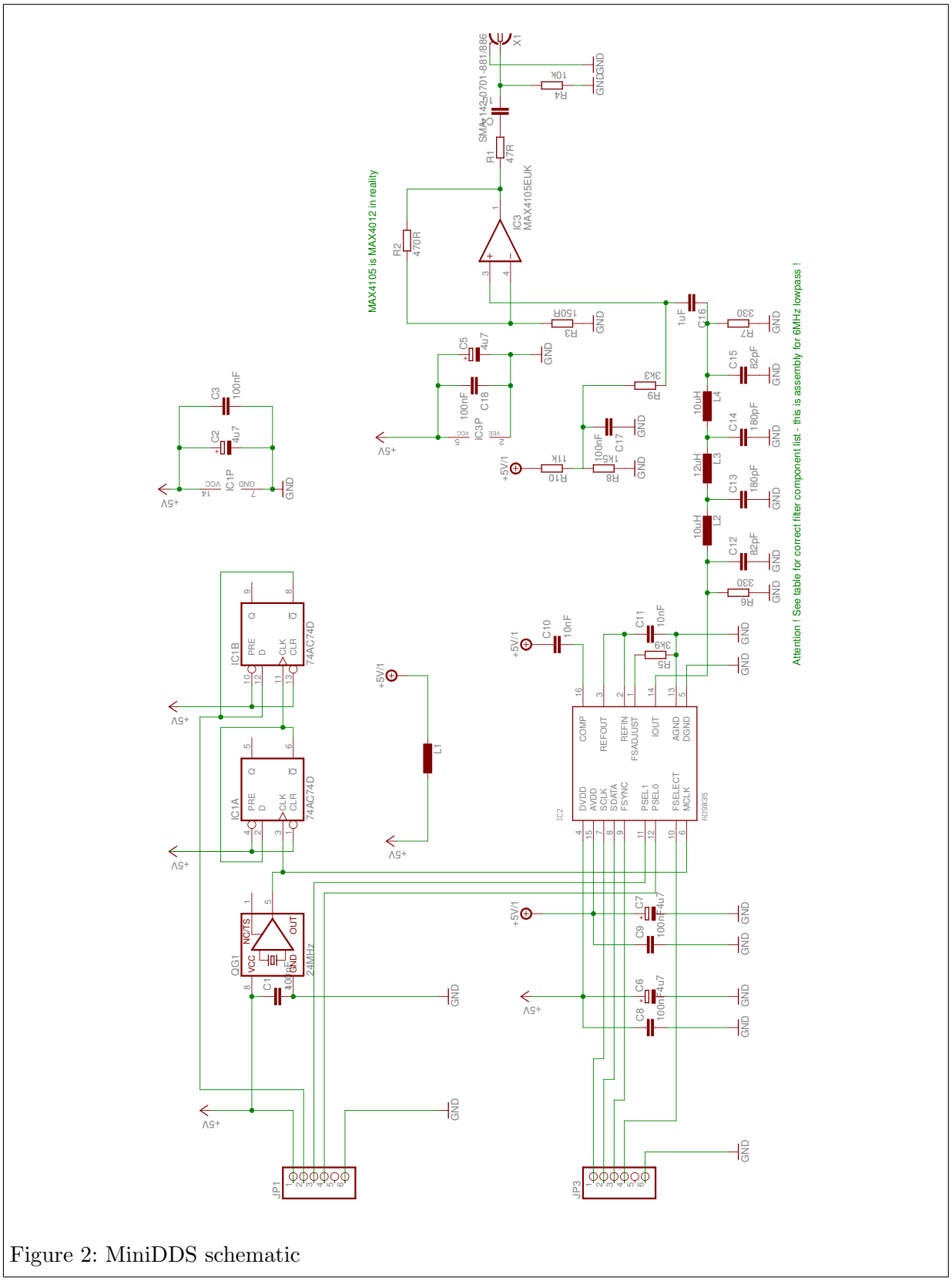

Figure 2: MiniDDS schematic

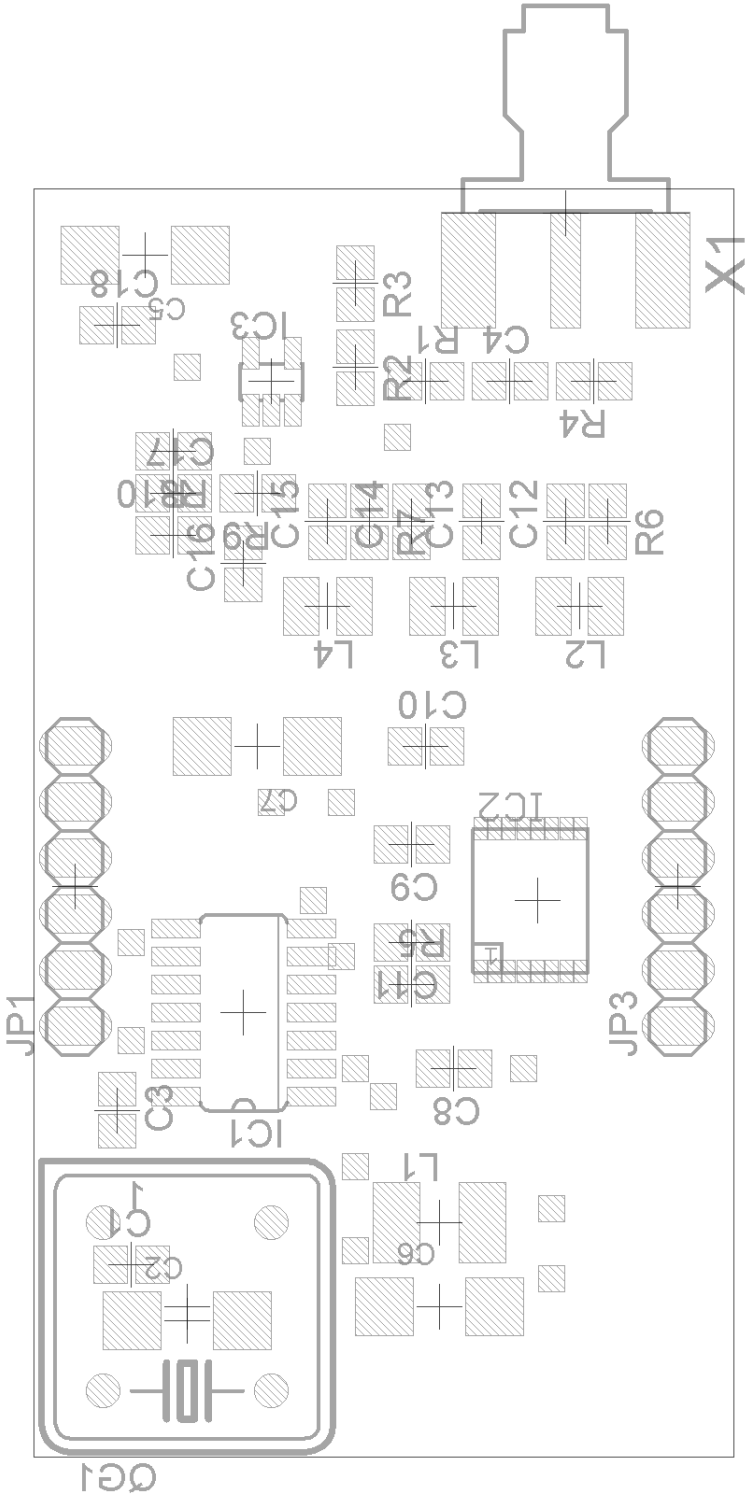

Figure 3: MiniDDS assembly plan

11 Further pictures

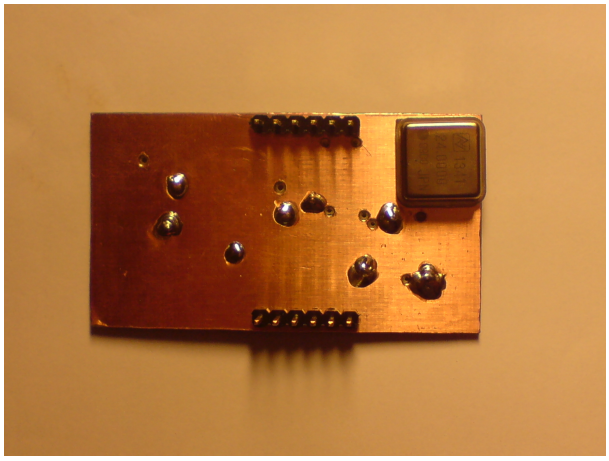

Figure 4: Bottom view of MiniDDS signal generator

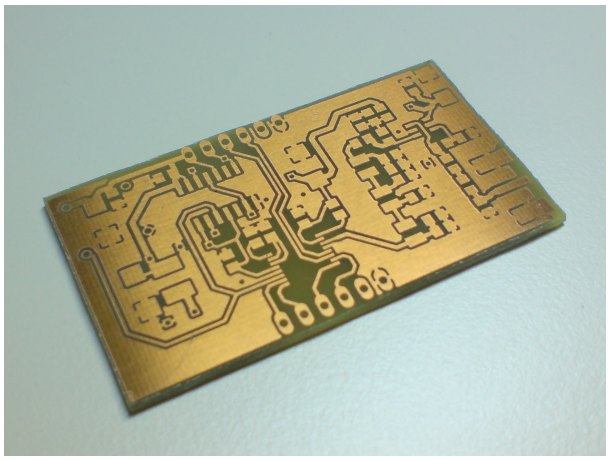

Figure 5: Unassembled PCB of MiniDDS signal generator